Cont'd
cont'd

19. The method of claim 16, further comprising switching another clock source to said input of said PLL in response to said control signal.

20. The method of claim 19, wherein said switching to said other clock source includes switching from a bus received clock source to a local clock source.

REMARKS

This Amendment and Response is filed in reply to the Office Action dated October 10, 2002. In this Response, Applicant amends claims 1, 14, and 15 to correct antecedent basis and form issues. Support for the amendments can be found throughout the originally filed disclosure. Cancellations of and/or amendments to the claims are not an acquiescence to any of the rejections. Furthermore, silence with regard to any of the Examiner's rejections is not an acquiescence to such rejections. Specifically, silence with regard to Examiner's rejection of a dependent claim, when such claim depends from an independent claim that Applicant considers allowable for reasons provided herein, is not an acquiescence to such rejection of the dependent claim(s), but rather a recognition by Applicant that such previously lodged rejection is moot based on Applicant's remarks and/or amendments relative to the independent claim (that Applicant considers allowable) from which the dependent claim(s) depends. Furthermore, any cancellations of and amendments to the claims are being made solely to expedite prosecution of the instant application. Applicant reserves the option to further prosecute the same or similar claims in the instant or a subsequent application. Upon entry of the Amendment, claims 1-20 are pending in the present application.

The issues of the October 10, 2002, Office Action are presented below with reference to the Office Action.

With regard to the Office Action, paragraphs 1-7: Examiner rejected claims 1 and 14 under 35 U.S.C. 112, second paragraph.

Applicant amends claims 1 and 14 to correct the typographical error cited by the Examiner, and to recite "said feedback filter circuit" instead of "said PLL filter circuit".

Further, Applicant respectfully disagrees with the Examiner's association of terms in independent claims 1 and 14. To assist the Examiner, Applicant provides carriage returns and spacing for the feature of "a phase-locked loop circuit ("PLL") having an input coupled to said switch output, and a frequency output, said PLL including a feedback filter circuit".

Based on the aforementioned amendments and comments, Applicant traverses Examiner's rejections of claims 1 and 14 under 35 U.S.C. 112.

With regard to the Office Action, paragraphs 8-24 and 33-40: Examiner rejected claims 1-4, 7, and 10-14 under 35 U.S.C. 102(e) as being anticipated by Bedrosian (U.S. Patent 5,740,211).

With specific reference to paragraph 15 of the Office Action, Applicant respectfully disagrees with the Examiner's characterization of Bedrosian with respect to Applicant's independent claim 1. Applicant's independent claim 1 recites "feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry *selectively coupling* at least one circuit element to said feedback filter circuit, wherein said selective coupling is *controlled by said clock detection circuit output*".

In contrast, Bedrosian does not teach *feedforward circuitry selectively coupling at least one circuit element to said feedback filter circuit*. Rather, Bedrosian teaches pulse aligning and pulse blocking circuitry connected to a phase comparator for causing the PLL's controlled oscillator to increase or decrease in frequency (Bedrosian, col. 7 lines 5-17). Pulse blocking circuitry is used to decrease the frequency of the input clock or the output clock by a factor of two (Bedrosian, col. 4 line 45 - col. 5 line 4), and the pulse aligning circuitry is used to sense the phase difference between the input sync signal and the output signal from the 1/N pulse circuit (Bedrosian, col. 5 line 57 - col. 6 line 56). Nowhere in Bedrosian is there taught *feedforward circuitry selectively coupling at least one circuit element to a PLL feedback filter circuit*.

Applicant also directs Examiner to the Office Action, page 4, last line of paragraph 15, where Examiner fails to provide a reference to Bedrosian in which Bedrosian teaches Applicant's claimed feature that includes: "said selectively coupling is controlled by said clock detection circuit output." Applicant also directs Examiner to Bedrosian, Column 4, lines 42-45, in which Bedrosian states: "The switching selection is controlled by either input failure monitors or by a manual command (*not shown*)." Examiner equates such statement with a teaching of Applicant's claimed feature of "a clock detection circuit", where Applicant's claim further states

that such clock detection circuit is coupled to the multiplexer selection input to select a clock input, and Examiner quotes the aforementioned passage from Bedrosian (see Office Action, page 3) in making such comparison. Applicant notes, however, that after such aforementioned passage, Bedrosian makes no further reference to such input failure monitor. Bedrosian thus also does not teach at any time, the feature of Applicant's independent claim 1 that such clock detection circuit output also controls the selectively coupling of the feedforward circuitry to the feedback filter circuit. As mentioned previously, Examiner does not provide a reference to Bedrosian with respect to this claimed feature, as such feature is not taught by Bedrosian.

Accordingly, because Bedrosian does not teach all features of Applicant's independent claim 1, and because Examiner failed to provide reference in Bedrosian for rejection of each of Applicant's claimed features, Applicant traverses Examiner's rejection of independent claims 1, and considers independent claim 1 to be allowable. Claims 2-13 depend from allowable independent claim 1, and are also allowable.

Applicant again directs Examiner to the Office Action, page 4, last line of paragraph 15, where Examiner fails to provide a reference to Bedrosian that teaches Applicant's claimed feature that includes: "said selectively coupling is controlled by said clock detection circuit output." If the aforementioned remarks are not considered as placing independent claim 1 in condition for allowance, Applicants request that a subsequent non-final Office Action provide a reference for the rejection of said claimed feature.

Because independent claim 14 also includes a feature of "feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said PLL filter circuit, wherein said selective coupling is controlled by said clock detection circuit output," for the reasons provided herein relative to Applicant's independent claim 1, Applicant submits that Bedrosian does not teach all features of Applicant's independent claim 14. Accordingly, Applicant traverses Examiner's rejection of independent claim 14 and considers independent claim 14 to be allowable.

With regard to the Office Action, paragraphs 25-26: Examiner rejected claim 15 under 35 U.S.C. 102(b) as being anticipated by Fazakerly et al. (U.S. Patent 4,208,635)

Independent claim 15 is amended to include language more consistent with the disclosure to recite "a detection circuit coupled to said clock source and having an output *representative of a presence of said clock source*".

In contrast, Fazakerly et al. do not teach a detection circuit coupled to a clock source and having an output *representative of a presence of the clock source*. Rather, Fazakerly et al. teach a phase detector that generates an output signal (V_{in}) that is proportional to the phase error between an oscillator signal frequency and an input reference signal frequency. (Fazakerly et al., col. 2 lines 45-60) Fazakerly et al. do not teach that the output signal V_{in} represents the presence of a clock source as claimed by Applicant in independent claim 15.

As provided previously herein with respect to independent claims 1 and 14, independent claim 15 also includes a detection circuit, the output of which couples a feedforward detection circuit to a feedback loop of a PLL. Such feature is not taught by Fazakerly et al. or Bedrosian.

Accordingly, Applicant traverses Examiner's rejection of independent claim 15 under 35 U.S.C. 102(b) and considers independent claim 15 to be allowable.

With regard to the Office Action, paragraphs 27-32: Claims 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Richards et al. (U.S. Patent 6,178,207). Applicant respectfully disagrees with the Examiner's characterization of Richards et al. with respect to Applicant's independent claim 16.

As filed, independent claim 16 recites "detecting a failure of said clock source" and "applying a control signal to said PLL in response to said failure of said clock source, said control signal altering a time constant within said PLL".

In contrast, Richards et al. do not teach *detecting a failure of a clock source* and *applying a control signal to alter a time constant within a PLL in response to a clock source failure*. Rather, Richards et al. teach a time constant that is based on a user determined factor *m* (Richards et al., col. 13 lines 7-67). Richards et al. accordingly do not detect a clock source failure and adjust a time constant, per Applicant's independent claim 16.

Accordingly, Applicant traverses Examiner's rejection of independent claim 16 under 35 U.S.C. 102(c) and considers independent claim 16 to be allowable. Claims 17-20 depend from independent claim 16 and are allowable as depending from an allowable base claim.

Conclusion

Applicant considers the Response herein to be fully responsive to the referenced Office Action. Based on the above Remarks, it is respectfully submitted that this application is in condition for allowance. Accordingly, allowance is requested. If there are any remaining issues or the Examiner believes that a telephone conversation with Applicant's attorney would be helpful in expediting the prosecution of this application, the Examiner is invited to call the undersigned at 617-832-1241.

Respectfully submitted,

Date: January 10, 2003

Kevin A. Oliver
Reg. No. 42,049

Foley Hoag LLP
World Trade Center West
155 Seaport Boulevard
Boston, MA 02210

Phone: 617-832-1000
Fax: 617-832-7000

MARKED-UP VERSION OF CLAIMS

1. (Once Amended) A clock circuit comprising:

first and second clock sources;

a multiplexer having a first input coupled to the first clock source, a second input coupled to the second clock source, and an output selectively couplable to said first and second inputs;

a clock detection circuit having an output representing a presence of said first clock source;

said multiplexer having a selection input coupled to said clock detection circuit output such that said multiplexer selects said first clock source as its output when said first clock source is present;

a phase-locked loop circuit ("PLL") having

an input coupled to said multiplexer output, and

a frequency output,

said PLL including a feedback filter circuit; and

feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said [PLL] feedback filter circuit, wherein said selective coupling is controlled by said clock detection circuit output.

14. (Once Amended) A system comprising:

multiple clock sources;

a switch having multiple inputs, said multiple inputs being respectively coupled to said multiple clock sources;

a clock detection circuit having an output representing a presence of one of said multiple clock sources;

said switch having a selection input coupled to said clock detection circuit output such that said switch selects one particular clock source of said multiple clock sources as its output when said one particular clock source is present;

a phase-locked loop circuit ("PLL") having

an input coupled to said switch output, and

a frequency output,

said PLL including a feedback filter circuit; and

feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said [PLL] feedback filter circuit, wherein said selective coupling is controlled by said clock detection circuit output.

15. (Once Amended) A circuit comprising:

a clock source;

a PLL circuit having said clock source as its input;

a detection circuit coupled to said clock source and having an output [responsive to] representative of a presence of said clock source; and

a feedforward correction circuit coupled to said output of said detection circuit and to a feedback loop of said PLL.